Optical spectroscopy of defects in nm-scale high-\(k\) dielectric and silicon-on-insulator (SOI) films

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Nanometer-scale high-\(k\) dielectric and SOI films have enabled devices to continue operating with high-speed and low power consumption...

... but are susceptible to formation of defects

“Faster, non-destructive ways of detecting these defects are needed.” ITRS 2009
Co-workers

Si/SiO₂/Hf₁₋ₓSiₓO₂

SOI

Sematech

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- Robert Welch Foundation
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Jimmy Price
PhD 2009

Ming Lei

Gennadi Bersuker

Pat Lysaght
A University-Industry Collaboration

The University of Texas at Austin
Founded 1886
www.utexas.edu

Sematech’s Albany, NY facility
Founded 2008
www.sematech.org
PROBLEM:
As \( d \rightarrow 1 \) nm, 
\[ I_{\text{leakage}} \rightarrow 100 \text{ A/cm}^2 \]
because of quantum tunneling
\[ \downarrow \]
power loss & heating, esp. in cell phones, laptops

SOLUTION:
Maintain high \( C = k\varepsilon_0 A/d \), for high device performance by replacing
\[ k_{\text{SiO}_2} = 3.9 \]
with
\[ 18 < k_{\text{Hf-silicate}} < 30 \]

A decade of intensive materials research preceded the commercial introduction of Hf-based dielectrics
Numerous obstacles were overcome before Hf-based oxides became a manufacturable solution for today’s chip industry.

<table>
<thead>
<tr>
<th>SiO₂</th>
<th>vs. Hf-based oxides</th>
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<tbody>
<tr>
<td>• Low density of defects</td>
<td>• High density of intrinsic defects</td>
</tr>
<tr>
<td>• Amorphous</td>
<td>• Susceptible to crystallization</td>
</tr>
<tr>
<td>• minimum dangling bonds</td>
<td>• Low quality SiO₂ interface</td>
</tr>
<tr>
<td>• Stable w/ poly Si gate.</td>
<td>• Elemental diffusion w/ metal gate</td>
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Further scalability depends on developing **non-invasive** methods for characterizing **intrinsic** & **process-induced** defects.
What are dielectric defects and how do they affect device performance

• Defects: anything that can trap an electron.
  - $O_2$, $N_2$, vacancies and / or interstitials
  - Impurities (C, B, etc.)
  - Crystal imperfections (grain boundaries, surface states)
  - All are discrete localized states within the band gap

• How does this affect device performance?
  - Charge trapping and $V_t$ instability
  - Increase in leakage current
  - Degradation of carrier mobility
Atomic Layer Deposition (ALD) was critical to integrating high-$k$ dielectric layers into commercial devices


**Benefits of ALD:**

- Atomic level control of film composition
- Uniform thickness over large areas
- Very smooth surfaces
- High density, minimal defects
- Low deposition temperature.
We have employed two complementary optical methods for identifying defects in Si/SiO$_2$/Hf$_{1-x}$Si$_x$O$_2$ structures.

**Spectroscopic Ellipsometry**

*(i.e. absorption)*

HfO$_2$-induced SiO$_2$ defects

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**Internal PE + EFI-SHG**

*(EFI = Electrostatic-Field-Induced)*

Tunable incident fs laser pulse


Both methods are fast, non-invasive, defect-specific & compatible with in-line metrology; neither requires device fabrication.
The need for non-invasive high-\(k\) defect metrology has driven an extension of SE methodology & application...

...from traditional role: characterizing thickness & broad-band \(\varepsilon(\omega)\) of ultra-thin films

...to new role: identifying **weak, discrete, sub-high-\(k\)-gap** absorption features relevant to electrical performance of high-\(k\) devices

\[\text{• relies on traditional parametrized } \varepsilon(\omega) \text{ models for Si substrate & bulk of SiO}_2, \text{ HfO}_2 \text{ layers}\]

\[\text{• absorption coefficient near discrete feature must be extracted using point-by-point data inversion methods}\]

\[\text{• artifacts from Si substrate CPs can appear if parametrized } \varepsilon(\omega) \text{ models are incorrect}\]

\[\text{e.g. because of strain, electrostatic fields, etc.}\]

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Sancho-Parramon *et al.*, TSF **516**, 7990 (2008)
We also observe Takeuchi’s 4.75 eV absorption peak + “ghosts” of Si $E_1$, $E_2$ and $E_1'$ critical points ...

+ additional peaks at 2.9, 3.6 and 3.9 eV

... but they all vanish when Si substrate replaced with SiO$_2$

⇒ the optically active defects cannot be in bulk HfO$_2$

Are they Si/SiO$_2$ defects? ⇒ remove the HfO$_2$ layer to find out
3 of 4 absorption peaks persist in absence of HfO$_2$

Peak height dependence on $t_{\text{SiO}_2}$ tracks $N_{it}$ derived from electrical data

- 1$^{\text{st}}$ spectroscopic identification of sub-gap defects in Si/SiO$_2$
- 4.75 eV peak:
  - noticeably absent, suggesting it’s HfO$_2$-induced.
  - also absent with Hf$_{1-x}$Si$_x$O$_2$ and Al$_2$O$_3$ overlayers, showing it’s HfO$_2$-specific
Peak amplitudes (but not energies) are sensitive to the high-\(k\) dielectric overlayer.

**Ab-initio calculations:**

*Ab initio* calculations predict that *oxygen vacancies* possess sub-SiO\(_2\)-gap optical transitions at energies close to the observed peaks.
Identification of sub-gap absorption peaks with O vacancies suggests a connection with \( V_{\text{flat band}} \) roll-off in high-\( k \) devices.

- \( V_{\text{fb}} \) in Si/SiO\(_2\)/high-\( k \) devices is observed to “roll off” quickly for \( t_{\text{SiO2}} < 3 \) nm.

[\( V_{\text{fb}} \) also varies in well-documented ways with anneal treatment, electrode work function, high-\( k \) material, etc.]

- \( V_{\text{fb}} \) variability leads to irreproducibility in device performance.

- A widely-accepted model* attributes \( V_{\text{fb}} \) variations to creation of oxygen vacancies in the SiO\(_2\) interfacial layer due to oxygen gettering by the high-\( k \) overlayer.

- O vacancies created in the thinnest SiO\(_2\) layers, where strained SiO\(_x\) dominates, are preferentially positively charged.

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2.9 eV peak closely tracks $V_{fb}$ dependence on $t_{SiO2}$

3.6, 3.9, and 4.75 eV peaks are less sensitive to $t_{SiO2}$

Results suggest 2.9 eV peak originates from positively-charged O-vacancies at the Si/SiO$_2$ interface that are responsible for $V_{fb}$ roll-off.
Intentional deposition of O-deficient HfO$_2$ film* simultaneously strengthens O-gettering & sub-gap absorption

* by reducing duration of O$_3$ pulse during ALD

- 2.9 eV peak doubles in strength in OD-HfO$_2$ sample because of enhanced O-gettering.

- 3.6, 3.9, 4.75 eV peaks strengthen by smaller fractions.

- Corresponding variations in $V_{fb}$ and ESR spectra are observed.
Sub-gap absorption gives immediate feedback on influence of processing steps on electrical properties, and correlates with known dependencies of $V_{fb}$ roll-off

J. Price, PhD dissertation (2009)

RTA = Rapid Thermal Anneal*

FGA = Forming Gas Anneal**

F implant into Si/SiO$_2$ interface before high-$k$ deposition***

* RTA contributes to $V_{fb}$ roll-off

** FGA helps passivate Si/SiO$_2$ interface defects

** F-implant suppresses $V_{fb}$ roll-off

Choi et al., IRPS 2007
In-situ feedback from optical monitor can help find process sequences that improve device performance

J. Price, PhD dissertation (2009)

D$_2$(a): low temp/pressure deuterium anneal
D$_2$(b): high temp/pressure deuterium anneal
D$_2$(b) + ALD of 3 nm HfO$_2$ almost completely suppresses 2.9 eV peak!

Unfortunately, the 2.9 eV recovers after a post-deposition anneal (PDA)
Internal multi-photon photoemission & time-dependent EFISH* are widely used to investigate charge trapping at oxide surfaces


*Electrostatic-Field-Induced Second Harmonic (EFISH) generation:
(1) Incident fs pulse 3-photon-excites electrons above SiO₂ CB barrier
(2) Electrons drift to oxide surface
(3) Electron trapping, catalyzed by ambient O₂, creates electrostatic field

For a narrow band of incident photon energies, we observe delayed EFISH decay in samples with as-grown HfO$_2$ films.
Time-dependent FDISH* measurements show no variation in SHG phase during scan

\[ I_{2\omega}(t) \propto \left| \chi^{(2)} \right| + \left| \chi^{(3)} \right| e^{i\Phi(t)} E_{DC}(t) \left| E_{\omega} \right|^2 \]

This rules out the possibility that EFISH decay is destructive interference between \( \chi^{(2)} \) and monotonically growing \( \chi^{(3)} E_{DC}(t) e^{i\Phi(t)} \)

* Frequency-Domain Interferometric Second-Harmonic (FDISH)

Resonant EFISH decay depends quadratically on incident power ...

... indicating it is induced by 2-photon excitation of transition with $2h\nu_{\text{laser}} = 3.2$ eV

... placing the ground state below the Si VB maximum
The photo-ionized defect ground state takes several hours to refill from the Si VB ...

... indicating the defects are located ≥ 1 nm into the HfO₂ bulk

\[ \tau_{\text{tunnel}} \approx 10^{-6} \text{s} \]

\[ \tau_{\text{tunnel}} \approx 10^4 \text{s} \]
EFISH decay is not observed for Si/SiO$_2$/Hf$_{1-x}$Si$_x$O$_2$ nor annealed Si/SiO$_2$/HfO$_2$ film stacks.

Optical methods enable detection of defects prior to processing (e.g. annealing, device fabrication)
Ab-initio calculations identify an oxygen vacancy defect in m-HfO$_2$ with an optical transition energy of $\sim$ 3.27 eV

- $V^0$, $V^+$ most stable defects (and highest oscillator strength)
- m-HfO$_2$ exists as small polymorphs in as-grown HfO$_2$, but absent in HfSiO
Summary of defects identified optically in Si/SiO$_2$/HfO$_2$ for the first time

<table>
<thead>
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<th>Defect Energy [eV]</th>
<th>Location</th>
<th>Nature</th>
<th>Method</th>
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<tr>
<td>2.9</td>
<td>Si/SiO$_2$ interface</td>
<td>Oxygen vacancy; responsible for $V_{fb}$ roll-off</td>
<td>SE</td>
</tr>
<tr>
<td>3.2</td>
<td>HfO$_2$ bulk</td>
<td>Oxygen vacancy; HfO$_2$-specific; removed by annealing</td>
<td>SHG</td>
</tr>
<tr>
<td>3.6</td>
<td>SiO$_2$</td>
<td>Intrinsic to Si/SiO$_2$</td>
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<td>4.75</td>
<td>SiO$_2$</td>
<td>Oxygen vacancy; HfO$_2$-induced HfO$_2$-specific</td>
<td>SE</td>
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</tbody>
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**Current work: with high-k, who needs silicon?**

\[\mu_n = 1350 \text{ cm}^2/\text{V}\]

\[\mu_n = 12000 \text{ cm}^2/\text{V}\]
Since IBM introduced it in 1998,* SOI has entered the mainstream of high-performance electronics & photonics ...


SOI MOSFETS

SOI waveguides & MEMS

[Diagram of SOI MOSFETS and waveguides]


Reed, Knights, Silicon photonics: an introduction (Wiley 2004)

... everyday life

... and high-end computing

[Images of Toyota Prius, Wii, and petaflop computers]
SOI provides advantages over conventional ICs at 2 levels...


**IC level: superior transistor isolation**

* conventional ICs: p-n junction isolation* → parasitic capacitance, limited transistor density


**SOI: dielectric isolation**

Each transistor is isolated from the Si substrate and from every other transistor by the BOX below, and by oxides above & on the sides

**Device level: alleviate “short channel” effects**

* conventional ICs: $E_{gate}$ competes with $E_{source-drain}$ ⇒ $V_{threshold}$ roll-off, reduced reliability

  Source-Drain leakage grows ⇒ high power consumption

* SOI: thin fully-depleted (FD) Si channel on insulator alleviates both problems

**ITRS 2005**

LSTP = Low Stand-by Power

LOP = Low Operating Power

HP = High Performance

**Threshold Voltage (Vt)**

**Gate Length (Lg)**

**Source-Drain Leakage**
Preparing an ultrathin single-crystal Si film on an amorphous insulator is a challenging problem:

Several competing technologies & companies have emerged to solve it:

**SIMOX**: Separation by IMplantation of OXygen

**Wafer Bonding**: Smart Cut™ from Soitec
Layer Transfer from SiGen
ELTRAN from Canon  

**Seed Methods**: Si layer grown directly on chemically-treated or crystalline insulator

Our samples were prepared by Plasma-Activated Wafer Bonding

SOI layer must be chemically thinned for final device prep.
During thermal oxidation thinning, defects created at the external surface migrate to the SOI/BOX interface ...


Defect density $N$ increases as $t_{SOI}$ thins, but how?

Linearly? Super-linearly?

Crystal-Oriented-particles (COPs) formed during CZ growth

Si vacancy or O precipitate formed during SOI thinning

... where they become performance-limiting charge traps
We reveal some SOI/BOX interface defects (destructively) by HF dipping (the standard diagnostic)


Optical micrographs of “punch-through” defects in 10, 7, 4 and 2 nm SOI films after HF soaking

“Faster, non-destructive ways of detecting these defects are needed.” ITRS 2009
We use internal PE + SHG to detect trapping of hot carriers in ultrathin ($t_{SOI} < 10$ nm) films

Lei et al., Appl. Phys. Lett. 96, 241105 (2010)
Quantitative analysis of TD-EFISH reveals defect density at SOI/BOX interface increases linearly as $t_{SOI}$ thins.

$$N(t_{SOI}) = \eta(D-t_{SOI}) + N_0$$

$t_{SOI} = 4 \text{ nm}$

$\lambda_{laser} = 750 \text{ nm}$

$P_{avg} = 150 \text{ mW}$

$E_2(t) \propto q_{trapped}(t) \propto 1 - e^{-t/\tau} + \text{ small correction}$

$$I_{2\omega}(t) \propto |\chi^{(2)} + \chi^{(3)}E_2(t)|^2 \propto |p_0 + (1 - e^{-t/\tau}) e^{i\Phi}|^2$$

$$\tau^{-1} \propto N(t_{SOI}) \Rightarrow \tau \propto N^{-1}(t_{SOI})$$

$$\propto \frac{1}{N_0 + \eta D} \left[ 1 + \frac{\eta t_{SOI}}{N_0 + \eta D} \right] + \ldots$$

for $\eta t_{SOI} \ll N_0 + \eta D$

(valid for ultrathin SOI)
Power-dependence shows SOI/BOX interface defect levels are excited by a two-photon process ...

... and thus lie $\geq 1$ eV below SiO$_2$ CB edge

But spectral dependence is weak for $1.5 \leq h\nu_{\text{laser}} \leq 1.7$ eV; no sharp resonant features observed.
SUMMARY

Epi-optics provides one answer to the clarion call of ITRS 2009:

“Faster, non-destructive ways of detecting these defects are needed.”

Price et al., JVST-B 27, 310 (2009)
Price et al., APL 95, 053906 (2009)
Lei et al., APL 96, 241105 (2010)
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