Characterization of strain fields around Through-Silicon Vias by second-harmonic scanning microscopy

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Overview: The semiconductor industry has traditionally followed Moore’s Law by downsizing devices and scaling integrated circuits in 2D. TSVs open up the third dimension.

Figure 1: Optical microscope image of top view of 3D cross-section of a TSV sample.

3D integration is a forefront technique for achieving high transistor density while reducing inter-chip RC delay and power consumption. “Through-Silicon Vias” (TSVs) achieve 3D integration by interconnecting vertically stacked devices. These short vertical interconnects enable better electrical performance and consume less power than longer interconnects needed in 2D integration. Cu is widely used as the TSV material because it is compatible with back-end-of-line processes, and has favorable electrical and mechanical properties. However, the large mismatch in coefficients of thermal expansion between Cu and Si induces thermal stresses during fabrication, testing and operation of TSV structures that can induce defects that degrade carrier mobility within the strain field surrounding TSVs. Here we show that scanning SHG microscopy is sensitive to these strain fields. Even though SHG is forbidden to lowest order from centrosymmetry, we observe a ~3 µm wide annulus around TSVs that is enhanced by strain.


Results. SHG is altered in a ~3 µm wide annulus around the TSVs in all polarization configurations: we observe (a) isotropic alteration in p-in/p-out and s-in/s-out configurations, and (b) anisotropic enhancement in p-in/s-out and s-in/p-out configurations. In the latter case, the anisotropic pattern rotates with the incident plane.

Discussion. Far from the TSVs, SHG originates from an isotropic surface polarization \( P_{surf}^{iso} \) and anisotropic bulk quadrupole polarization \( P_{bulk}^{iso} \cos 4\theta \). Near the TSVs, an anisotropic strain-induced polarization \( P_{strain}^{iso}(\phi) \) also contributes.

Acknowledgment. This work was supported by the Robert Welch Foundation.

Farbod Shafiei et al. Optics of Surfaces and Interfaces (OSI 2013) – Chemnitz/Germany