Scanning Capacitance Microscopy

“Nanostructure characterization techniques”

UT-Austin
PHYS 392 T, unique # 59770
ME 397 unique # 19079
CHE 384, unique # 15100

Instructor:
Professor C.K. Shih

Lecture Note: 11/06/09
Scanning Capacitance Microscopy

- A brief review of C-V characteristics of MIS devices
- Early days of SCM
- Scanning Capacitance Spectroscopy
- Role of tip-induced band bending
- Scanning depletion microscopy
- SCM of Devices in operation
- 2D dopant profiling (best results by 2004)
References

- APL 55, 1664 (1989)
- APL 72, 698 (1998)
- APL 74, 272 (1999)
- APL 74, 3672 (1999)
- APL 75, 2319 (1999)
- RSI 70, 158 (1999)
- JVST B18, 549 (2000)
- RSI 74, 127 (2003)
- RSI 75, 422 (2004)
Capacitance vs Bias

Accumulation

- Dielectric
- SCM Probe
- N-type Semiconductor

Depletion

- SCM Probe
- N-type Semiconductor

Bias Voltage

Capacitance

Accumulation
- Higher concentration
- ΔC

Depletion
- Lower concentration
- ΔC
- ΔV
SCM Setup

- Laser Detector
- Laser
- Conducting Probe
- Sample
- X-Y Stage
- Scanner
- Computer
- SPM Control Electronics
- SPM Head Electronics
- UHF Resonant Capacitance Sensor
- Capacitance Measurement Electronics
- Transmission Line
- DC Bias & AC Modulation Voltages
SCS SETUP

Laser Detector

Laser

Conducting Probe

Scanner

Sample

X-Y Stage

Computer

SPM Control electronics

Capacitance Measurement Electronics

Programmable DC bias

AC Modulation

Transmission Line

AC Modulation
Inception of SCM
[APL 55, 203 (1989)]

Scanning capacitance microscopy on a 25 nm scale

C. C. Williams, W. P. Hough, and S. A. Rishton
T. J. Watson Research Center, IBM, Yorktown Heights, New York 10598

(Received 13 February 1989; accepted for publication 2 May 1989)

A near-field capacitance microscope has been demonstrated on a 25 nm scale. A resonant circuit provides the means for sensing the capacitance variations between a sub-100-nm tip and surface with a sensitivity of $1 \times 10^{-19}$ F in a 1 kHz bandwidth. Feedback control is used to scan the tip at constant gap across a sample, providing a means of noncontact surface profiling. Images of conducting and nonconducting structures are presented.
The Key to SCM: RCA capacitance sensor

Schematic of the RCA sensor

RCA resonance circuit,
Resonant frequency 915 MHz
Q ~ 20 to 40

Sensitivity: \( \sim 10^{-21} \) F (early days only \( 10^{-19} \) F)
Lateral dopant profiling with 200 nm resolution by scanning capacitance microscopy

C. C. Williams, J. Slinkman, W. P. Hough, and H. K. Wickramasinghe
T. J. Watson Research Center, IBM, Yorktown Heights, New York 10598

Measurement of dopant density in silicon with lateral resolution on the 200 nm scale has been demonstrated with a near-field capacitance technique. The technique is based upon the measurement of local capacitance between a 100 nm tip and a semiconducting surface. Lateral dopant imaging is achieved by the measurement of the voltage-dependent capacitance between tip and sample due to the depletion of carriers in the semiconductor, as the tip is scanned laterally over the surface. Measurements of dopant density have been demonstrated over a dopant range of $10^{15}$ to $10^{20}$ cm$^{-3}$. Capacitance-voltage measurements have been made on a submicrometer scale.

APL 55, 1664 (1989)
SCM for dopant profiling
$dC/dV$ across a dopant grating
C-V measurements across the dopant grating

Comparison with the theory (1D simulation)
dC/dV image across the edge of the dopant grating
Scanning capacitance spectroscopy: An analytical technique for pn-junction delineation in Si devices

Hal Edwards, Rudye McGlothlin, Richard San Martin, Elisa U., and Michael Gribelyuk
Components and Materials Research Center, Texas Instruments, Inc., Dallas, Texas 75265

Rachel Mahaffy and C. Ken Shih
Department of Physics, The University of Texas at Austin, Austin, Texas 78712

R. Scott List and Vladimir A. Ukrain'tsev
Silicon Technology Development, Texas Instruments, Inc., Dallas, Texas 75265

(Received 8 October 1997; accepted for publication 9 December 1997)

Scanning capacitance spectroscopy (SCS), a variant of scanning capacitance microscopy (SCM), is presented. By cycling the applied dc bias voltage between the tip and sample on successive scan lines, several points of the high-frequency capacitance–voltage characteristic \( C(V) \) of the metal–oxide–semiconductor capacitor formed by the tip and oxidized Si surface are sampled throughout an entire image. By numerically integrating \( dC/dV \), spatially resolved \( C(V) \) curves are obtained. Physical interpretation of the \( C(V) \) curves is simpler than for a \( dC/dV \) image as in a single-voltage SCM image, so that the \( pn \) junction may be unambiguously localized inside a narrow and well-defined region. We show SCS data of a transistor in which the \( pn \) junction is delineated with a spatial resolution of \( \pm 30 \) nm. This observation is consistent with the conclusion that SCS can delineate the \( pn \) junction to a precision comparable to the Si depletion width, in other words, the actual size of the electrical \( pn \) junction. A physical model to explain the observed SCS data near the \( pn \) junction is presented. © 1998 American Institute of Physics. [S0003-6951(98)03206-9]
• Interleave positive/negative bias in subsequent line scans (reducing offset of C-V due to charging, e.g. -0.25, 0.25, -0.5, 0.5, -0.75, 0.75.
• Record phase and magnitude of $dC/dV$
• Integrate $dC/dV$ to obtain C-V curve
• $dC/dV$ obtained from lock-in amplifier. Modulation amplitude 1 – 2V.

FIG. 1. SCS data of a 0.6 $\mu$m, N-channel MOS field-effect transistor. Image size is $(2 \times 1) \mu$m$^2$. (a) amplitude $|dC/dV|$ and (b) phase $\Theta\{dC/dV\}$ images at a tip bias voltage of 0.25 V. Source, drain, substrate, and gate (white rectangle) are labeled in (a). Movement of the $pn$-junction signature under applied bias voltage may be seen in the phase images (c)–(e).
FIG. 2. (a)–(c) Schematic of carrier movement in Si near the *pn* junction with a biased tip above the Si oxide surface. (d) Qualitative summary of tip–sample capacitance at different tip locations.
FIG. 3. Methods to visualize the $pn$ junction. (a) A map of the voltage at which the $C(V)$ curve has a minimum. White is purely $p$ type and black is purely $n$ type. (b) $(300 \times 150)$ nm$^2$ zoomed image from the gray box in (a), with the $C(V)$ curve plotted within each $(15 \text{ nm})^2$ pixel.
Quantification of scanning capacitance microscopy imaging of the $pn$ junction through electrical simulation

Lucent Technologies, Bell Laboratories, Murray Hill, New Jersey 07974

APL 74, 272 (1999)

FIG. 1. Schematic of SCM analysis showing a one-dimensional scan of an electrode over a $pn$ junction with a 2 nm oxide deposited on top. The characteristic $C-V$ and $dC/dV-V$ curves for each material type are indicated.
FIG. 2. SCM images for a 150 nm gate length device. The images are 750×750 nm. At $V_{\text{bias}} = +1.5$ V, a small channel region is seen. As $V_{\text{bias}}$ is decreased the channel region increases until it is not discernable. The positive $dC/dV$ regions represent the $n$-type source and drain while the channel has a negative $dC/dV$ indicative of $p$-type material.
FIG. 5. Simulation data for a *pn* junction. (a) Electrode placed over the *n*-type region: at $-2$ V the electrons under the electrode are depleted, the holes are accumulated and there is a potential drop across the depletion region. (b) Electrode placed over the *n*-type region: the electron concentration changes as the electrode bias is changed from $-2$ to $2$ V. (c) Electrode placed over the depletion region: the real position of the *pn* junction moves as the electrode bias is changed from $-2$ to $2$ V.
Scanning depletion microscopy
[APL 74, 3672 (1999)]

Electrical simulation of scanning capacitance microscopy imaging of the pn junction with semiconductor probe tips

Lucent Technologies, Bell Laboratories, Murray Hill, New Jersey 07974

(Received 25 January 1999; accepted for publication 21 April 1999)
FIG. 2. Contour plots of the hole concentrations of $n$- and $p$-type samples probed with $p$-type silicon tips are shown. The relationship between $V_{\text{bias}}$ and the charge distribution in the sample and the tip can be clearly seen. For tip and sample of different carrier type, majority carriers are depleting and accumulating at the same $V_{\text{bias}}$, respectively. If the tip and sample have the same carrier type the opposite occurs.
FIG. 6. SCM micrographs of a 60 nm n-MOS transistor scanned with a boron-doped silicon cantilever tip. The LDD, HDD, channel, and gate are all clearly visible. There is little change in the contrast from image to image over a 1 V range; something not seen in images obtained with metal probe tips.
SCM of Device in Operation

Observation of metal–oxide–semiconductor transistor operation using scanning capacitance microscopy

C. Y. Nakakura, a) D. L. Hetherington, M. R. Shaneyfelt, and P. J. Shea
Microelectronics Development Laboratory, Sandia National Laboratories, Albuquerque, New Mexico 87185

A. N. Erickson
Digital Instruments, Santa Barbara, California 93117

(Received 29 April 1999; accepted for publication 11 August 1999)

We report scanning capacitance microscopy (SCM) images of a working p-channel metal–oxide–
semiconductor field-effect transistor (P-MOSFET) during device operation. Independent bias
voltages were applied to the source/gate/drain/well regions of the MOSFET during SCM imaging,
and the effect of these voltages on the SCM images is discussed. © 1999 American Institute of
Physics. [S0003-6951(99)03241-6]

APL 75, 2319 (1999)
FIG. 1. (a) Schematic diagram of the cross sectioned, 0.5 μm P-MOS test structure used in this study. The gate oxide thickness is 120 Å, and the retrograde n-well doping is $3 \times 10^{17}$ cm$^3$ at the well surface. (b) Drawing of the device layout showing the location of the active region in relation to the 100 μm x 100 μm bond pads.
FIG. 2. A $I-V$ curve of the cross-sectioned P-MOS device collected just prior to SCM imaging ($V_D = -5.0$ V and $V_S = V_W = 0$ V). The nanoampere leakage current in the cross-sectioned device increased from the prepolishing range of picoamperes.
FIG. 3. Images of the P-MOS device obtained simultaneously using: (a) AFM and (b) SCM. The topographical image (a) shows the gate structure at the top of the image, as well as the Ti–silicide contacts on either side of the gate (dark regions delineated with dashed lines). The SCM image (b) shows the carrier concentration profile, revealing the \( p^+ \) implanted source and drain, \( n \)-type well, and \( p^- \) type epitaxial layer.
SCM images of a P-MOS with $V_D = -3.0$ V, $V_S = V_W = 0$ V, and $V_G =$ (a) 0 V, (b) -1.75 V, and (c) -3.0 V. The sequence shows the formation of a conduction path between source and drain as the gate voltage is scanned.
Method for the study of semiconductor device operation using scanning capacitance microscopy

C. Y. Nakakura, a) P. Tangyunyong, D. L. Hetherington, and M. R. Shaneyfelt
Microelectronics Development Laboratory, Sandia National Laboratories, Albuquerque, New Mexico 87185

(Received 2 August 2002; accepted 17 October 2002)

A new method for studying semiconductor device operation with cross-sectional scanning capacitance microscopy (SCM) is described. The technique uses a modified, commercial SCM system to image device cross sections while dc voltages are incrementally applied to bias test structures between nonconducting and conducting states. The novel test structure design and packaging simplify sample preparation while enabling the application of voltages to discrete regions of the semiconductor device. By recording sequential SCM images as a function of bias voltage, the process of switching a device “off” and “on” can be visualized to study carrier movement in the active region of the device. Two sample SCM sequences of metal–oxide–semiconductor field-effect transistors, one fabricated on a bulk silicon substrate and the other on a silicon-on-insulator substrate, are presented to show typical carrier movement in these devices. © 2003 American Institute of Physics. [DOI: 10.1063/1.1527722]
Schematic of the SCM measurement of the cross section of a $p$-channel, bulk Si MOSFET. The diagram of the sample shows the $p^+$ source and drain implanted in an $n$ well. An external function generator applies the capacitance-modulating bias to the tip, while an external lock-in amplifier monitors the output of the capacitance sensor. The HP-4145 semiconductor parameter analyzer provides dc bias voltages for the device and also measures the device current. The device to the package leads are coated with epoxy for protection while handling.
FIG. 2. (a) Drawing of the test structure layout showing the location of the active region of the device in relation to the 100 μm x 100 μm bond pads. The dotted line is parallel to the cross-sectioned edge of the prepared sample. (b) Photograph of the mounted and packaged SCM sample. The test structure shown in (a) is circled and is mounted hanging off the edge of the package to allow access to the cross section for polishing. Bond wires connecting the device to the package leads are coated with epoxy for protection while handling.
FIG. 3. (a) Photograph of the modified polish stub next to a SCM sample. The socket plate contains spring-loaded pins that accept the SCM sample and is fixed to the face of a standard polish stub. (b) Photograph of the sample mounted in the polish stub. The tapped holes are used to mount two clamping bars (not pictured), which hold the sample rigidly in place.
FIG. 4. Plot of drain current as a function of the polish step during sample preparation of a bulk Si, \( p \)-channel MOSFET. The off-state current was taken from \( I-V \) curves (measured with \( V_D = -0.1 \) V; \( V_S = V_W = 0 \) V) at \( V_G = 1 \) V. The dotted line denotes the first step where the device was exposed at the cross section, determined by both top-down and cross-sectional measurements with an optical microscope.
FIG. 5. Photograph of the SCM sample mounted in the test fixture during a SCM measurement. The packaged sample is shown at the center with the SCM tip in position over the cross-sectioned edge. Electrical signals from the HP-4145 are routed to the device via the group of wires in the bottom-right of the photo to the connector on the PCB. The test fixture is recess mounted in the vacuum chuck of the AFM.
FIG. 6. (Color) Sequence of SCM images of the bulk Si, p-channel test structure with $V_D = -0.1$ V, $V_S = V_W = 0$ V, and $V_G = (a) 0$, (b) $-1.05$, and (c) $-1.75$ V. The progression of the SCM images shows the formation of a conducting channel between the source and drain. The schematic drawing in (a) shows the approximate locations of the polysilicon gate, titanium nitride spacers, the titanium silicide contacts. The arrow in (a) denotes the region of color banding referred to in the text. Images were acquired with $V_{ac} = 2.0$ V peak to peak and $V_{dc} = 0$ applied to the SCM tip.
FIG. 7. An $I_D-V_G$ curve of the bulk Si, $p$-channel test structure generated from point-by-point electrical measurements recorded while performing SCM measurements ($V_D = -0.1$ V, $V_S = V_W = 0$ V). The large, shaded circles labeled (a), (b), and (c) correspond to the sequence of SCM images shown in Fig. 6.
FIG. 8. Current–voltage ($I_D$ vs $V_G$) curves for the bulk Si, $p$-channel test structure recorded (a) as a function of cross sectioning, and (b) as a function of the lighting environment with the cross-sectioned sample mounted in the SCM. The $I–V$ curves for the illuminated cases in (b) were recorded with the tip in scanning position. For all the $I–V$ curves, $V_D = -0.1$ V and $V_S = V_W = 0$ V.
FIG. 9. Schematic of the cross section of a BUSFET structure fabricated on a SOI substrate. The $n^+$ drain is formed by a deep implant that extends down to the buried oxide layer, whereas the $n^+$ source is formed by a shallow implant, allowing a conduction path between the $p$ body and $p^+$-body contact.
FIG. 10. (Color) Sequence of SCM images of an n-channel BUSFET, recorded with $V_D=0.1$ V, $V_S=V_{body}=0$ V, and $V_G$ = (a) 0, (b) 0.4, and (c) 0.75 V. The SCM sequence shows the formation of the conduction path between the source and drain. The schematic drawing in (a) shows the approximate locations of the polysilicon gate, titanium nitride spacers, and titanium silicide contacts. The dotted line beneath the source/drain denotes the silicon/buried oxide interface. Images were acquired with $V_{ac}=1.0$ V peak to peak and $V_{dc}=0$ applied to the SCM tip.
FIG. 11. $I_D$ vs $V_G$ curve of the $n$-channel BUSFET generated from in situ electrical measurements recorded while recording SCM images ($V_D = -0.1$ V, $V_S = V_{Body} = 0$ V). The large, shaded circles labeled (a), (b), and (c) are $I-V$ measurements for the images shown in Fig. 10.
Importance of the sample surface preparation

Polishing, cleaning, and only native oxide

Heating (300 C) under UV exposure

FIG. 2. Cross-sectional SCM images in the vicinity of a p-n junction, left-hand side after polishing with colloidal silica suspension, and right-hand side after low temperature heating under UV exposure.
Sub-10 nm SCM resolution

Sub-10 nm lateral spatial resolution in scanning capacitance microscopy achieved with solid platinum probes

E. Bussmann and C. C. Williams

Department of Physics, University of Utah, 115 S 1400 E, Room 201, Salt Lake City, Utah 84112

(Received 15 September 2003; accepted 26 October 2003)

FIG. 1. (a) SEM image of the usual tip geometry. (b) The small scale (~10 nm) geometry of the tip imaged by SEM. A circle of 19.92 nm diameter is shown as a scale to aid the eye.
FIG. 2. Images of a 70 nm gate length SOI FET device. (a) The sample has been held at a dc bias of $-2 \text{ V}$ with respect to the flatband voltage and the apparent electrical junctions around the source/drain extensions shift inward. (b) The sample has been held at $+1 \text{ V}$ with respect to the flatband potential and the source/drain extensions recede.
FIG. 3. The discrete SCM sampling over the transition region from the SOI layer (left) to channel region (right). The measured SCM is the mean of ten individual measurements to suppress noise. The transition length is in agreement with that simulated for a 5 nm tip. The dotted vertical line indicates the junction between the SOI layer (left) and the doped channel region (right).
FIG. 4. (a) Measured SCM and simulated SCM for 8.5 nm radius tip on sample 1 ($n^+/p$, 24 nm junction depth). The simulation calculates capacitance based on the dopant profile, so it becomes inaccurate in the junction region where the carrier and dopant profiles diverge. The simulation predicts an apparent electrical junction (SCM zero signal crossing) very near the metallurgical junction depth (~24 nm). (b) The overlain SIMS and SCM dopant profiles. The spike in the SCM profile near the left edge is a consequence of the slightly lower SCM signal measured near the edge due to the influence of the $a$-Si layer there. The spike in the center of the SCM profile (~29 nm depth) is a consequence of the SCM conversion model which is not adequate to handle the junction.
FIG. 5. (a) Measured SCM and simulated SCM (10 nm tip radius) for the four step boron epitaxial staircase structure with $\sim 75$ nm steps. The resolution in this case is not as high as expected for a sub-10 nm tip radius, probably due to both larger tip radius and rf voltage. (b) The SCM dopant profile and SIMS profile for the epitaxial staircase sample.
FIG. 5. Impact of the tip model on the spatial resolution simulated for SEMATEC No. 1 sample in \( \Delta V \) mode.
FIG. 6. Time average band bending underneath the hemispherical tip with radius $R_t=35$ nm calculated in small signal approximation $V_{rf}=0$ V and for amplitude of probing signal $V_{rf}=2$ V. The oxide thickness is $t_{ox}=20$ Å and silicon doping concentration is $N_D=10^{15}$ cm$^{-3}$. 